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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,775	MABUCHI, KEIJI	
	Examiner	Art Unit	
	DENNIS HOGUE	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11,13-18 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11,13-18 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the fourth Office Action based on the 10/673,775 application filed 9/29/2003. Claims 6-11, 13-18, and 20-27 are currently pending and have been considered below. Claims 1-5, 12, and 19 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 6-11, 13-18, and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

Remarks

3. There are several problems with the most recent claim amendments. Firstly, they are only supported in the context of the first embodiment ("First Example" in the specification) and the third embodiment ("Third Example"). That is, the claim amendments recite subject matter of the first embodiment that does not apply to the second embodiment. For this reason, claims 8, 15, and 22 are rejected under USC 112, and, in the examiner's opinion, should be cancelled. Further, the independent claims define that the plurality of pixels are pixels in a pixel row, but the dependent claims define that the plurality of pixels are arranged in a two-dimensional array. These statements are contradictory. In short, the dependent claims need to be put into form consistent with the amended independent claims.

4. Regarding the subject matter of the most recent amendments, and taking claim 6 as an example, the amendments appear to be directed to subject matter of the first embodiment shown in Fig. 4. Fig. 4 shows that each row of pixels in the pixel array is formed in a separate well. In the specification, the term "well region" is used to refer to an individual well. However, in the claims, apparently with the intention of making the independent claims generic to all disclosed embodiments, the term "well region" does not refer to an individual well, but rather to a region containing one or more wells. This must be the case in view of claim 9. However, this interpretation of the language makes the claims much easier to reject because the examiner needs only to draw an imaginary dotted line around whatever contains the well in a given reference and call that region a "well region", including whatever else within that region that is helpful for rejecting the claim. In the examiner's opinion, it would be better to use the term "well region" in a manner similar to its use in the specification, where it refers to a particular well. See for example, page 22 of the specification, which discloses that the well regions 200 of Fig. 4 correspond to P-wells, and the pixel section 110 comprises multiple well regions 200.

That is, the claims currently refer to a well region as some arbitrary region that contains a well (e.g. such as the box delineated by element 110 in Figs. 4 and 6), where later in claim 8 the well region is further defined to be a contiguous well, and in claim 9 the well region is further defined to be a region containing several non-contiguous wells, which the examiner points out, requires the well region to contain sub-regions that are not wells. In the examiner's opinion, this was likely done so that the well region of claim 6 would be generic to the both embodiments 1 and 2. However, especially in view of the latest amendment which places subject matter in the independent claims directed to embodiment 1 that is not a feature of embodiment 2, it would be better to set forth that the well region is one of the well regions 200 in Fig. 4, and not a region around all of the well regions 200 as it currently must be construed in view of the entire claim set.

To do this, the Applicant could set forth that the semiconductor substrate has a plurality of well regions formed thereon, wherein each well region of the plurality of well regions is electrically isolated from other well regions of the plurality of well regions. Further, to better define the relationship of the well regions to the pixel unit, the applicant could define that the pixel unit has a plurality of pixel rows on the semiconductor substrate, each pixel row comprising a plurality of pixels formed in one of the well regions of the plurality of well regions. Still further, to better indicate that the items (a) through (d) are elements of each pixel in a particular row and formed in the same well region, the applicant could define that for a first pixel row of the plurality of pixel rows, each pixel in the plurality of pixels includes (a) a photoelectric conversion element formed in a first well region of the plurality of well regions to... and so on. The

examiner is not saying that this alone would make the claim allowable, but it would more effectively define the concept shown in Fig. 4 and at least limit the art that the examiner can use to reject the claim.

Consider the current claim language which states that the semiconductor substrate comprises a well region, a plurality of pixels in a pixel row have a photoelectric conversion element and a readout section formed in the well region, and the well region is electrically isolated from other well regions along the row. Rhodes (US 6,825,878) teaches a CMOS image sensor where the imaging array is formed in a first well, and the peripheral circuitry is formed in a second well, with the advantage that the threshold voltages of the MOS transistors can then be separately optimized for each section. This reference teaches the new limitations because the current claim language does not even require that the other well regions are part of the pixel unit.

5. Further, regarding claim 6, in the examiner's opinion, "dependent upon the read out of the signal charge by said readout section" is not particularly specific, and does not adequately describe the inventive concept of the first two embodiments. The inventive concept is that the substrate voltage is changed when the charge is read out by the transfer transistor. The operation of image sensors is cyclical, and therefore in the examiner's opinion, any reference that comprises a voltage control unit to apply a variable substrate bias voltage to the well region at any point in the operational cycle can be construed to satisfy the current claim language. Neither does claim 27 capture the inventive concept because it simply defines that the application of the substrate bias voltage is synchronized with charge transfer. This does not require that the substrate bias voltage be applied at the same time as charge transfer. The language "the readout voltage is reduced" is not given much weight as the readout voltage is not even defined in claim 6. Based on the disclosure, the intent of this language is likely that the readout voltage is a signal voltage applied to the gate of the readout section. However, even though the claims are interpreted in light of the specification, aspects of the specification are not imported into the claims. In the current form, "the readout voltage" can be broadly interpreted, or even ignored, as it is unclear under USC 112 for lack of antecedent basis and definition.

Claim Objections

6. Claim 16 is objected to because of the following informalities: "cell" should be changed to "well". Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 8 recites subject matter directed to the 2nd embodiment of the invention ("Second Example"), whereas claim 6 from which it depends has been amended to include subject matter specifically directed the 1st embodiment of the invention ("First Example"). The features of the two embodiments are mutually exclusive. The claim requires the well region to include all of the pixels of the pixel unit, to be electrically integral, and to be electrically isolated from other well regions which in view of the specification include some of the pixels of the pixel unit. In the examiner's opinion, claim 8 should be cancelled in view of the most recent amendment to the claims.

9. Claims 15 and 22 are rejected under 35 U.S.C. 112, first paragraph, for similar reasons as claim 8.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 defines that the plurality of pixels comprises pixels in a pixel row. Claim 7 then defines that the plurality of pixels is a two dimensional array of pixels. These statements are contradictory. Further, claim 8 recites features that the well region is electrically integral and comprises all of the pixels of the two dimensional array, when claim 6 has already defined that the well region comprises pixels of a row and is electrically isolated from other wells, which in view of the specification, are wells comprising other rows of the two dimensional array of pixels. Claim 9 is indefinite because it depends from claim 7.

12. Claims 14-16 and 21-23 are rejected under 35 U.S.C. 112, first paragraph, for similar reasons as claims 7-9.

13. Claim 27 recites the limitation "the readout voltage is reduced". There is insufficient antecedent basis for this limitation in the claim. Further, what the readout voltage is has not been defined, so it is impossible to determine whether or not it has been reduced.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 6-8, 11, 13-15, 18, 20-22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) and Rhodes (US Patent 6,825,878).

Regarding claim 6, Murakami et al. teach a solid-state complementary metal-oxide semiconductor type image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39), comprising: a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A; further, any region of the semiconductor substrate comprising the P semiconductor region is a well region); and a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels in a pixel row on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (a) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (b) a readout section to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (drive transistor 212 or selection transistor 213 can be interpreted as readout sections, see Fig. 19A); (c) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A); and (d) a voltage control unit to apply a variable substrate bias voltage to said well region upon the read out of the signal charge by said readout section (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment

where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively; note that in all cases a different substrate voltage is applied when the pixel is not being exposed; therefore, the substrate voltage is varied, and a particular substrate voltage is applied when the pixel is read out; the substrate voltage is also applied to the well region because they are in contact, see Fig. 19A). However, Murakami et al. do not teach a readout section formed in said well region, or that the well region is electrically isolated from other well regions along the pixel row. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65), and the periphery logic transistors are formed in a separate well (col. 7 lines 62-65). This allows the threshold voltage of the transistors in each section to be optimized separately (col. 8 lines 20-25).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the threshold voltage of the transistors in each section to be optimized separately. This would improve the quality of the image sensor.

Regarding claim 7, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said plurality of pixels are arranged in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim 8, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 7, wherein said well region is electrically integral in a region of said

semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions (Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well, col. 7 lines 62-65).

Regarding claim 11, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6, wherein said solid-state image pickup device each pixel also includes a pixel transistor connected to said photoelectric conversion element through said node for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (Murakami et al. teach drive transistor 212, see Fig. 19A; Raynor et al. teach amplifying transistor M1, see Fig. 4; both of these transistors are pixel transistors for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line).

Regarding claim 13, Murakami et al. teach a complementary metal-oxide semiconductor type solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39), comprising: a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A; further, any region of the semiconductor substrate comprising the P semiconductor region is a well region); and a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (a) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (b) a readout section to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (drive transistor 212 or selection transistor 213 can be interpreted as readout sections, see Fig. 19A); (c) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (d) a voltage control unit to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate

voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively; note that in all cases a different substrate voltage is applied when the pixel is not being exposed; therefore, the substrate voltage is varied, and a particular substrate voltage is applied when the pixel is read out; the substrate voltage is also applied to the well region because they are in contact, see Fig. 19A). However, Murakami et al. do not teach a readout section formed in said well region, or that the well region is electrically isolated from other well regions along the pixel row. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65), and the periphery logic transistors are formed in a separate well (col. 7 lines 62-65). This allows the threshold voltage of the transistors in each section to be optimized separately (col. 8 lines 20-25).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the threshold voltage of the transistors in each section to be optimized separately. This would improve the quality of the image sensor.

Regarding claim 14, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 13, wherein said plurality of pixels are arranged in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim15, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 14, wherein said well region is electrically integral in a region of said

semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions (Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well, col. 7 lines 62-65).

Regarding claim 18, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 13, wherein said solid-state image pickup device each pixel also includes a pixel transistor connected to said photoelectric conversion element through said node for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line (Murakami et al. teach drive transistor 212, see Fig. 19A; Raynor et al. teach amplifying transistor M1, see Fig. 4; both of these transistors are pixel transistors for converting the signal charge read out from said photoelectric conversion element into an electric signal and outputting the electric signal to a signal line).

Regarding claim 20, Murakami et al. teach a method to drive a solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39) including (a) a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A; further, any region of the semiconductor substrate comprising the P semiconductor region is a well region) and (b) a pixel unit (multiple sensing means 2, Fig. 8) including a plurality of pixels in a pixel row on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (i) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (ii) a readout section to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (drive transistor 212 or selection transistor 213 can be interpreted as readout sections, see Fig. 19A); (iii) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A); and (iv) a voltage control means to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48;

Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively), said method comprising the steps of: converting light to a signal charge (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); storing said signal charge during a charge storage period (the electric charges are stored in the photodiode until such time that the selection transistor 213 is turned on by signal X, see Fig. 19A); and applying a predetermined substrate bias voltage to said well region that is variable dependent upon the signal charge read out by said readout section during said readout period (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively). However, Murakami et al. do not teach a readout section formed in said well region, or that the well region is electrically isolated from other well regions along the pixel row. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65), and the periphery logic transistors are formed in a separate well (col. 7 lines 62-65). This allows the threshold voltage of the transistors in each section to be optimized separately (col. 8 lines 20-25).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the threshold voltage of the transistors in each section to be optimized separately. This would improve the quality of the image sensor.

Regarding claim 21, Murakami et al. in view of Raynor et al. and Rhodes teaches the driving method for the complementary metal-oxide semiconductor type solid-state

image pickup device according to claim 20, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

Regarding claim 22, Murakami et al. in view of Raynor et al. and Rhodes teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 20, wherein said well region is electrically integral in a region of said semiconductor substrate which includes all of said pixels arranged in the two-dimensional array, and a common substrate bias voltage to all of said pixels is applied to the well regions (Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well, col. 7 lines 62-65).

Regarding claim 25, Murakami et al. teach a method for driving a complementary metal-oxide semiconductor type solid-state image pickup device (solid-state image sensing device 1 which is a CMOS sensing means, col. 5 lines 36-39) including (a) a semiconductor substrate (P- semiconductor region 221 is a substrate, see Fig. 19A) having a well region formed thereon (P semiconductor region 222 is a well region, Fig. 19A; further, any region of the semiconductor substrate comprising the P semiconductor region is a well region); and (b) a pixel unit (multiple sensing means 2, Fig. 8) having a plurality of pixels on the semiconductor substrate (multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8), each pixel in the pixel unit including (i) a photoelectric conversion element formed in said well region to receive light and produce a signal charge in accordance with an amount of the received light (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); (ii) a readout section to read out the signal charge produced by said photoelectric conversion element at a predetermined readout timing (drive transistor 212 or selection transistor 213 can be interpreted as readout sections, see Fig. 19A); (iii) a node connected to the photoelectric conversion element (a node connects the N semiconductor region 224 to drive transistor 212, see Fig. 19A), the node having a capacitance (any real electrical node has a capacitance with respect to any other real electrical node); and (iv) a voltage control unit to apply a substrate bias voltage to said well region and change the substrate bias voltage during a storage period of the signal charge by said photoelectric conversion element (the substrate

voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively), said method comprising the steps of: converting light to a signal charge (N semiconductor region 224 and P semiconductor region 222 form a photodiode, see Fig. 19A; as is well known in the art, the photodiode converts photons into electric charges); storing said signal charge during a charge storage period (the electric charges are stored in the photodiode until such time that the selection transistor 213 is turned on by signal X, see Fig. 19A); and applying a substrate bias voltage to said well region and changing the substrate bias voltage during said storage period of the signal charge by said photoelectric conversion element (the substrate voltage is varied during the exposure period so as to increase the dynamic range of the captured image, col. 5 lines 43-48; Fig. 9 shows an embodiment where the substrate voltage is varied during exposure, having two distinct substrate voltages that are applied; embodiments wherein the substrate voltage is varied in unequal time amounts, four different equally spaced levels, four logarithmically spaced voltage levels, and continuously varied are shown in Figs. 11, 13, 15, and 17 respectively). However, Murakami et al. do not teach a readout section formed in said well region, or that the well region is electrically isolated from other well regions along

the pixel row. That is, Murakami et al. teach the common three transistor (3T) CMOS pixel, which does not feature a transfer gate.

Raynor et al. teach a CMOS image sensor having the common four transistor (4T) pixel structure (see Fig. 4). Note that this structure differs from the three transistor structure (as shown in Fig. 1) in that a transfer gate transistor has been added (transistor M4). As is well known in the art, the pixel is read out by a timing signal Vtx applied to the gate of the transfer transistor M4. Raynor et al. teach that advantages of the 4T pixel structure over the 3T structure are increased sensitivity and that the 4T structure allows for a rolling shutter application (col. 1 line 58 to col. 2 line 9).

Therefore, it would be obvious to one of ordinary skill in the art to combine the transfer gate of Raynor et al. with the imaging device of Murakami et al. so that the sensitivity of the device could be improved and a rolling shutter application could be supported. This would increase the quality of the images captured by the camera device.

Rhodes teaches that all of the pixels of the pixel portion of an image sensor are formed in a single well (col. 7 lines 62-65), and the periphery logic transistors are formed in a separate well (col. 7 lines 62-65). This allows the threshold voltage of the transistors in each section to be optimized separately (col. 8 lines 20-25).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for the pixel array of Rhodes with the image sensor of Murakami et al. in view of Raynor et al. so that the threshold voltage of the transistors in each section to be optimized separately. This would improve the quality of the image sensor.

Regarding claim 26, Murakami et al. in view of Raynor et al. and Rhodes teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 25, wherein said photoelectric conversion element is provided for each of a plurality of pixels formed in a two-dimensional array on said semiconductor substrate (Murakami et al.: multiple sensing means 2 is arrayed in a matrix, col. 5 lines 24-26, see Fig. 8; the pixels are the individual sensor elements of Fig. 8).

16. Claims 9, 16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) and Rhodes as applied to claims 7, 14, and 21 above, and further in view of Chi (US Patent 6,501,109).

Regarding claims 9 and 16, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 7 and 14. However, Murakami et al. in view of Raynor et al. and Rhodes does not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Murakami et al. in view of Raynor et al. and Rhodes so that the well for each row could be individually pulsed for enhancement of the pixel dynamic range. This would increase the quality of images captured by the camera.

Regarding claim 23, Murakami et al. in view of Raynor et al. and Rhodes teaches the driving method for the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 21. However, Murakami et al. in view of Raynor et al. and Rhodes does not teach wherein said well region is formed in an electrically isolated relationship for each row of said pixels arranged in the two-dimensional array, and an independent substrate bias voltage is applied to the cell regions for each row.

Chi teaches a CMOS image sensor (col. 3 lines 40-41) wherein a row of pixels is constructed in a single well (col. 4 lines 8-9). Having a well for each row of pixels allows the well for each row to be individually pulsed for enhancement of the pixel dynamic range (col. 5 lines 62-65).

Therefore, it would be obvious to one of ordinary skill in the art to combine the single well for a row of pixels as taught by Chi with the image sensor of Murakami et al. in view of Raynor et al. and Rhodes so that the well for each row could be individually pulsed for enhancement of the pixel dynamic range. This would increase the quality of images captured by the camera.

17. Claims 10, 17, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) and Rhodes as applied to claims 6, 13, and 20 above, and further in view of Merrill (US Patent 5,747,840).

Regarding claims 10 and 17, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claims 6 and 13, wherein said well region is a p-type well region (Murakami: P semiconductor region 222 is a well region, Fig. 19A). However, Murakami et al. in view of Raynor et al. and Rhodes does not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one layer and a negative voltage to the other layer (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Murakami et al. in view of Raynor et al. and Rhodes so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

Regarding claim 24, Murakami et al. in view of Raynor et al. and Rhodes teaches the driving method for a complementary metal-oxide semiconductor type solid-state image pickup device according to claim 20, wherein said well region is a p-type well region (p-well 102). However, Murakami et al. in view of Raynor et al. and Rhodes does not teach that the substrate bias voltage is a negative voltage.

Merrill teaches a CMOS image sensor (col. 2 lines 26-28) wherein a photodiode 100 (Fig. 4) is formed in a p-well 112, 114 formed on a substrate 110 (substrate 110 may be n-type col. 4 lines 33-38). Merrill teaches that it is advantageous to reverse bias the well-substrate interface by applying a positive voltage to one and a negative voltage to the other (col. 1 lines 58-60) because the reverse biased junction prevents thermally generated carriers from diffusing from the substrate to the photodiode (col. 2 lines7-12). This improves the noise characteristics of the photodiode. Merrill further teaches that including a highly doped layer as a sub layer of the well will increase the quantum efficiency of the photodiode by deflecting photoelectrically generated charge carriers

back toward the photodiode that would otherwise be lost to the substrate (col. 3 lines 30-33).

Therefore, it would be obvious to one of ordinary skill in the art to combine the highly doped well sub layer and the reverse biased well-substrate junction of Merrill with the image sensor of Murakami et al. in view of Raynor et al. and Rhodes so that noise characteristics and quantum efficiency would be improved. This would increase the quality of the images captured by the sensor. In such a combination, a negative voltage would be applied to the p-well and a positive voltage would be applied to the n-substrate.

18. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US Patent 6,486,460) in view of Raynor et al. (US Patent 7,375,752) and Rhodes as applied to claim 6 above, and further in view of Nakagawa (Japanese Patent Application Publication 2000-022126).

Regarding claim 27, Murakami et al. in view of Raynor et al. and Rhodes teaches the complementary metal-oxide semiconductor type solid-state image pickup device according to claim 6. However, Murakami et al. in view of Raynor et al. and Rhodes does not teach wherein the readout voltage is reduced by applying the substrate bias voltage synchronized with charge transfer.

Nakagawa teaches an image sensor wherein when the charge is transferred from the photoelectric conversion device, a lower substrate voltage is applied to the substrate than the voltage applied to the substrate prior to transferring the charges (see

abstract). This reduces the voltage required at the transfer gate to transfer the charge and therefore reduces the power consumption of the device (see abstract).

Therefore, it would be obvious to one of ordinary skill in the art to combine the reduced substrate voltage at transfer of Nakagawa with the imaging device of Murakami et al. in view of Raynor et al. and Rhodes so that the power consumption of the device could be reduced. This would reduce heat in the sensor and also extend battery life.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS HOGUE whose telephone number is (571) 270-5089. The examiner can normally be reached on Mon. - Thurs., 8:00 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lin Ye/

Supervisory Patent Examiner, Art Unit 2622

DH

Examiner